What is claimed is:

[Claim 1] 1. A method for placing a plurality of electrostatic discharge (ESD) protection devices within an integrated circuit design, said method comprising:

defining a region within said integrated circuit design;

generating a list of ESD-susceptible circuits located within said defined region;

determining a preferred location for placing an ESD protection device within said region;

placing an ESD protection device at said determined location;

determining whether or not all ESD-susceptible circuits within said list of ESD-susceptible circuits are protected by the placement of said ESD protection device; and

generating a set of all ESD-susceptible circuits within said defined region and associating said set of all ESD-susceptible circuits with said ESD protection device if all ESD-susceptible circuits within said list of ESD-susceptible circuits are protected by the placement of said ESD protection device.

[Claim 2] 2. The method of Claim 1, wherein said method further includes dividing said region if not all ESD-susceptible circuits within said list of ESD-susceptible circuits are protected by the placement of said ESD protection device.

[Claim 3] 3. The method of Claim 1, wherein said method further includes reducing the number of ESD protection devices by removing redundant ESD protection devices.

[Claim 4] 4. The method of Claim 1, wherein said preferred location is the center of gravity of said ESD-susceptible circuits within said defined region.

[Claim 5] 5. The method of Claim 1, wherein said method further includes legalizing said placed ESD protection device at said determined location by satisfying physical requirements such as snapping to a grid and avoiding blockages.

[Claim 6] 6. The method of Claim 1, wherein said method further includes identifying all ESD-susceptible circuits within said integrated circuit design that cannot satisfy ESD requirements regardless of the number of ESD protection devices placed.

[Claim 7] 7. A computer program product residing on a computer usable medium for placing a plurality of electrostatic discharge (ESD) protection devices within an integrated circuit design, said computer program product comprising:

program code means for defining a region within said integrated circuit design;

program code means for generating a list of ESD-susceptible circuits located within said defined region;

program code means for determining a preferred location for placing an ESD protection device within said region;

program code means for placing an ESD protection device at said determined location;

program code means for determining whether or not all ESD-susceptible circuits within said list of ESD-susceptible circuits are protected by the placement of said ESD protection device; and

program code means for generating a set of all ESD-susceptible circuits within said defined region and associating said set of all ESD-susceptible circuits with said ESD protection device if all ESD-susceptible circuits within said list of ESD-susceptible circuits are protected by the placement of said ESD protection device.

[Claim 8] 8. The computer program product of Claim 7, wherein said computer program product further includes program code means for dividing said region if not all ESD-susceptible circuits within said list of ESD-susceptible circuits are protected by the placement of said ESD protection device.

[Claim 9] 9. The computer program product of Claim 7, wherein said computer program product further includes program code means for reducing the number of ESD protection devices by removing redundant ESD protection devices.

[Claim 10] 10. The computer program product of Claim 7, wherein said preferred location is the center of gravity of said ESD-susceptible circuits within said defined region.

[Claim 11] 11. The computer program product of Claim 7, wherein said computer program product further includes program code means for legalizing said placed ESD protection device at said determined location by

satisfying physical requirements such as snapping to a grid and avoiding blockages.

[Claim 12] 12. The computer program product of Claim 7, wherein said computer program product further includes program code means for identifying all ESD-susceptible circuits within said integrated circuit design that cannot satisfy ESD requirements regardless of the number of ESD protection devices placed.

[Claim 13] 13. A method for checking the effectiveness of a plurality of electrostatic discharge (ESD) protection devices placed within an integrated circuit design, said method comprising:

identifying all ESD-susceptible circuits within said integrated circuit design;

modeling each of said plurality of ESD protection devices associated with said ESD-susceptible circuits as a voltage source connected in series with a resistor;

modeling an ESD event striking on one of said ESD-susceptible circuits as a current source at said one of said ESD-susceptible circuits;

comparing a voltage on said one of said ESD-susceptible circuits during said ESD event to a predetermined voltage threshold;

in a determination that said voltage on said one of said ESD-susceptible circuits during said ESD event exceeds said predetermined voltage threshold, designating said one of said ESD-susceptible circuits as failing an ESD check.

[Claim 14] 14. The method of Claim 13, wherein said method further includes modeling a power distribution network of said integrated circuit design as a resistive network.

[Claim 15] 15. The method of Claim 13, wherein said method further includes using a linear circuit simulator to compute the voltage at said one of said ESD-susceptible circuits during said ESD event.

[Claim 16] 16. The method of Claim 13, wherein said method further includes providing a quantitative measure of failure for all of said ESD-susceptible circuits to enable efficient fix-up techniques.

[Claim 17] 17. A computer program product residing on a computer usable medium for checking the effectiveness of a plurality of electrostatic discharge (ESD) protection devices placed within an integrated circuit design, said computer program product comprising:

program code means for identifying all ESD-susceptible circuits within said integrated circuit design;

program code means for modeling each of said plurality of ESD protection devices associated with said ESD-susceptible circuits as a voltage source connected in series with a resistor;

program code means for modeling an ESD event striking on one of said ESD-susceptible circuits as a current source at said one of said ESD-susceptible circuits;

program code means for comparing a voltage on said one of said ESD-susceptible circuits during said ESD event to a predetermined voltage threshold;

in a determination that said voltage on said one of said ESD-susceptible circuits during said ESD event exceeds said predetermined voltage threshold, program code means for designating said one of said ESD-susceptible circuits as failing an ESD check.

[Claim 18] 18. The computer program product of Claim 17, wherein said computer program product further includes modeling a power distribution network of said integrated circuit design as a resistive network.

[Claim 19] 19. The computer program product of Claim 17, wherein said computer program product further includes program code means for using a linear circuit simulator to compute the voltage at said one of said ESD-susceptible circuits during said ESD event.

[Claim 20] 20. The computer program product of Claim 17, wherein said computer program product further includes program code means for providing a quantitative measure of failure for all of said ESD-susceptible circuits to enable efficient fix-up techniques.